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| **22bec121** |  |
| **Experiment – 5** | **Date:-7/2/2024** |

**Lab Work**

**Q1 .To design a and implement a 1024 x 8 ROM on FPGA .**

# Code (ROM)

// ROM

module sneh56 (

input [9:0]address ,

input enable ,

input clk ,

output reg [7:0]data

) ;

reg [7:0]memory[1023:0] ;

integer i ;

initial

begin

for (i = 0; i < 1024; i = i + 1) begin

memory[i] = i + 1;

end

end

always @(posedge clk)

begin

if (enable == 1)

begin

data = 0 ;

end

else

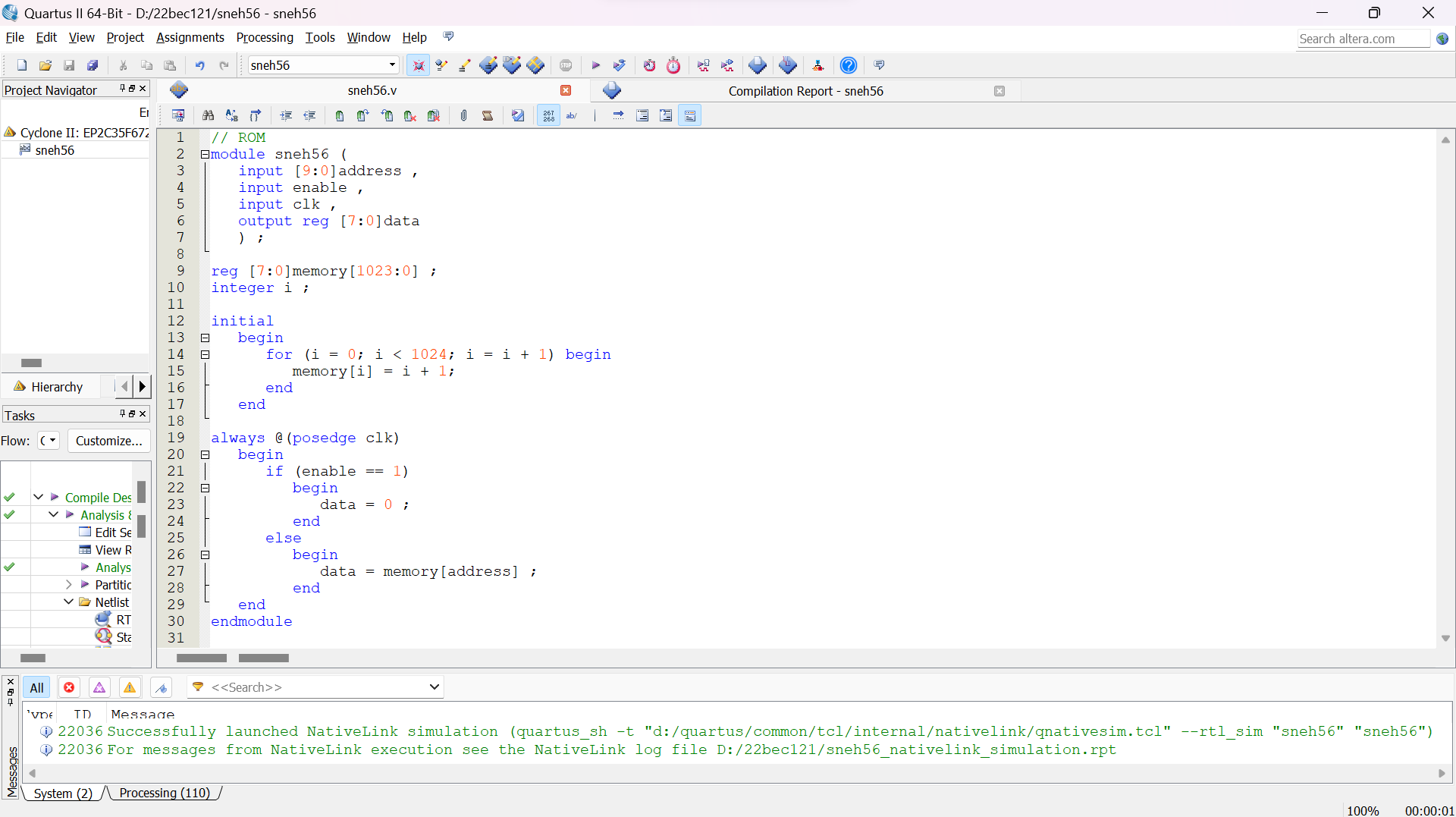
begin

data = memory[address] ;

end

end

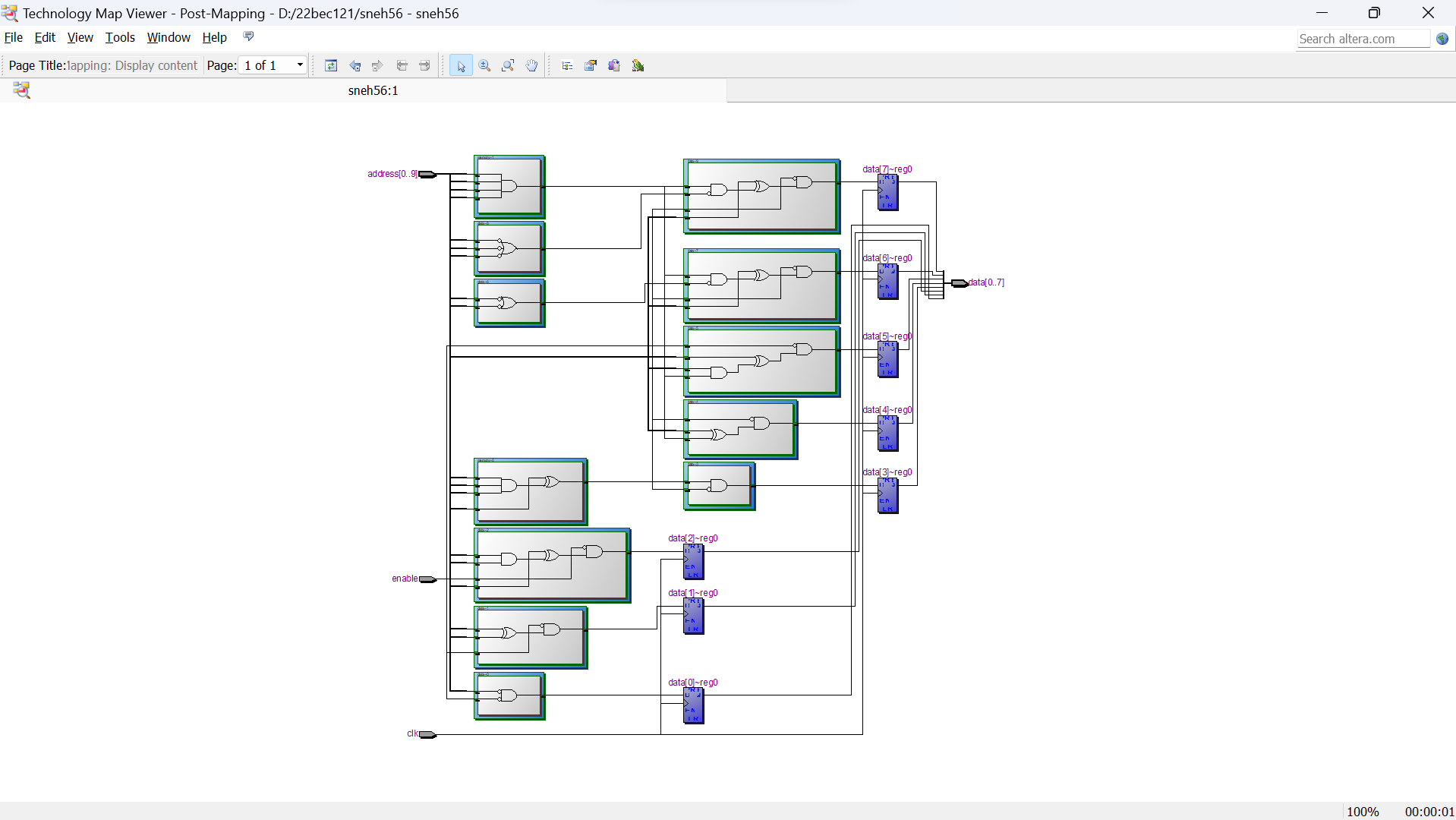
endmodule

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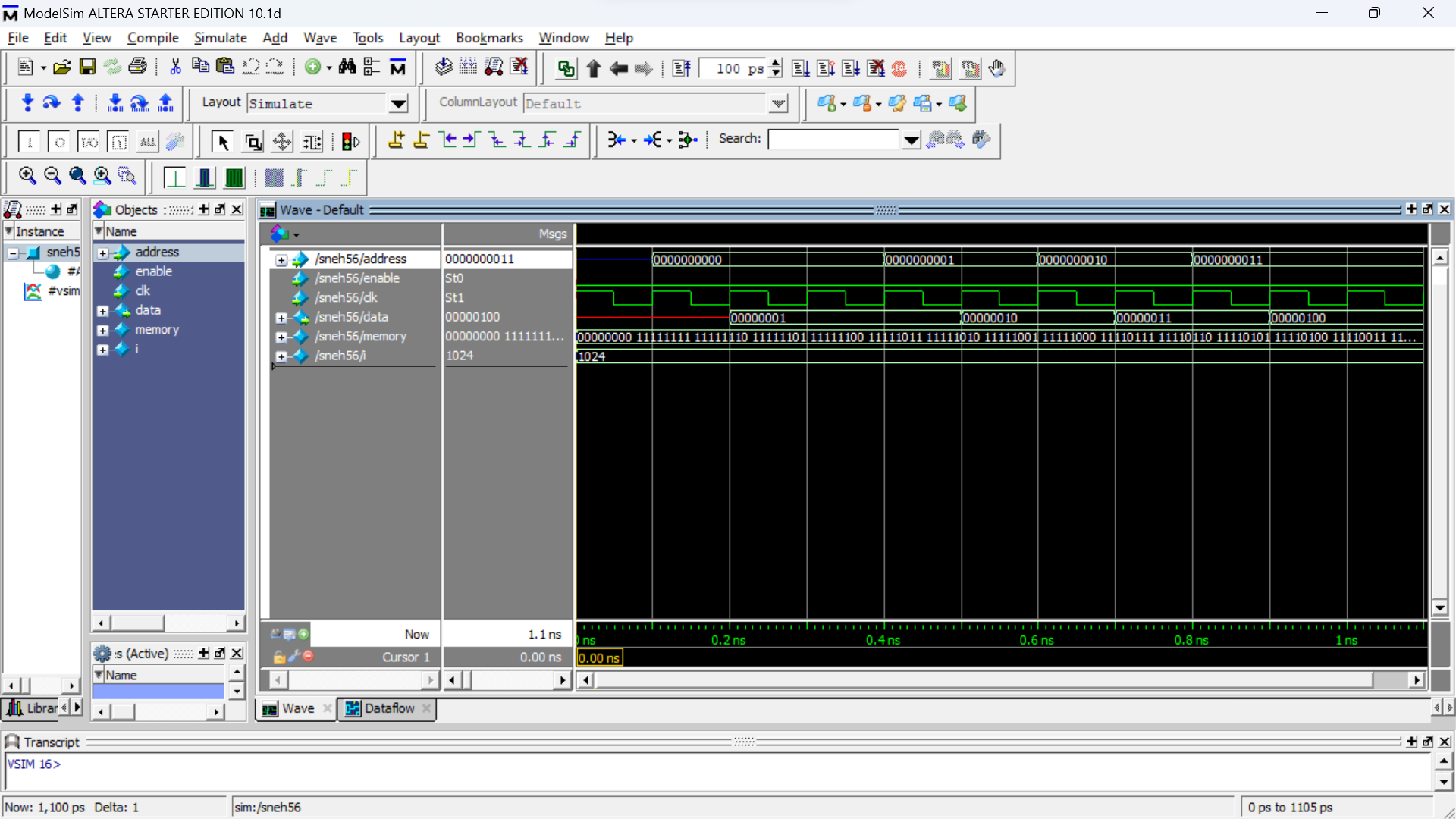
# Output 1)Cyclone II (RTL View)

# 

**2)Cyclone II (TTL View)**



**Simulation Results :-**

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**Conclusion :- In this experiment we learnt to design a 1024 x 8 ROM and the concepts of ROM in depth .**

**We also learnt that what is the RTL and TTL of a ROM and also verified it using the Simulation .**

**We also implemented ROM on a FPGA Kit . Also , we learned the different types of ROM used in Day – to – Day Scenarios .**